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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,898	04/06/2006	Shinji Watanabe	8017-1189	3401
466	7590	08/21/2008		
YOUNG & THOMPSON			EXAMINER	
209 Madison Street			LOUIE, WAI SING	
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ALEXANDRIA, VA 22314			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/574,898	Applicant(s) WATANABE ET AL.
	Examiner Wai-Sing Louie	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 June 2008.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 17-25,27,28,33,34,36 and 37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 17-25,27,28,33-34,36 and 37 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No./Mail Date 6/13/08
- 4) Interview Summary (PTO-413)
 Paper No./Mail Date _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

DETAILED ACTION

The argument in the response to the non-final rejection is persuasive and the non-final rejection of previous office action is withdrawn. A new ground of rejection is as below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 17-25, 27, 33-34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita (US Pub. 2002/0135057) in view of Matsumura (US Pub. 2003/0101584).

With regard to claims 17-18, Kurita discloses a semiconductor device (¶ [0028] et seq. and fig. 4) comprising:

- A wiring substrate 13 including an insulating resin layer 7 having a first major surface and a second surface 15 and a first wiring layer 14 disposed on the insulating resin layer 7 on the second major surface 15 side (¶ [0031], [0048] and fig. 4);
- A second wiring layer 3 formed on the first major surface of the insulating resin layer 7 (¶ [0031] and fig. 4);

- A chip 1 including a projection electrode 2 on a bottom surface and mounted on the wiring substrate 13 (¶ [0028] and fig. 2), where the insulating resin layer 7 holds the chip 1 such that a bottom and at least a part of side surfaces of the chip 1 are in contact with the insulating resin layer 7 (fig. 4), and a top surface of the chip 1 is exposed on the insulating resin layer 7 on the first major surface 15 side, and where the projection electrode 2 of the chip 1 is connected with the first wiring layer 3 (fig. 4);
- Kurita does not disclose the projection electrode 2 of the chip 1 having a sharp tip. However, Matsumura discloses the electrodes 18 have a sharp tip (Matsumura ¶ [0049] and fig. 5b). Matsumura teaches the sharp tip provides desirable contact with the electric parts (Matsumura ¶ [0006]). Therefore, it would have been obvious to one of ordinary skill in the art to modify Kurita's device with the teaching of Matsumura to provide a desirable contact with the electric parts.

With regard to claim 19, Kurita discloses a ground pattern is formed in the second wiring layer 3 (¶ [0036]).

With regard to claims 20-22, Kurita discloses a plurality of insulating resin layers 7 are laminated such that first major surfaces 15 are faced in the same direction for holding chip 1 and they are arranged on both surfaces of the wiring substrate 13 (fig. 3).

With regard to claims 23-24 and 33, in addition to the limitations disclosed in claim 17 above, Kurita also discloses:

- A wiring substrate 13 including a plurality of insulating resin layers 7 that are laminated (fig. 3) and have first major surfaces and second major surfaces 15 and

- a first wiring layer 14 disposed on the insulating resin layer 7 on the second major surface 15 side from a lowermost layer to an innermost layer in the insulating resin layers 7 (fig. 3);
- A second wiring layer 3 formed on the first major surface of the insulating resin layer 7 (fig. 3)

With regard to claims 25 and 34, Kurita discloses a portion exposed from the insulating resin layer 7 of the chip 1 that enters the insulating resin layer 7 pf the outermost layer in the wiring substrate 13 is covered by a coating resin (¶ [0008]).

With regard to claims 27 and 36, Kurita modified by Koyama disclose the projection electrode 12 is gold (Koyama ¶ [0056]).

Claims 28 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita (US Pub. 2002/0135057) in view of Sakamoto et al. (US 6,791,199).

With regard to claims 28 and 37, Kurita does not disclose the insulating resin is thermoplastic or thermosetting resin. However, Sakamoto et al. disclose the insulating resin could be a thermosetting resin (Sakamoto col. 4, lines 50-54). Sakamoto et al. teach the thermosetting resin could be molded, injected, dipped or painted on (Sakamoto col. 7, lines 6-10). Thus, it would have been obvious at the time the invention was made to modify Kurita's device with the teaching of Sakamoto et al. to use a thermosetting resin in order to be easily applied or formed.

Response to Arguments

Applicant's arguments with respect to claims 17-28 and 33-37 have been considered but are moot in view of the new ground(s) of rejection in view of newly cited reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is 571-272-1709. The examiner can normally be reached on 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

Wsl
August 15, 2008.